TABLE OF CONTENTS

Chairman's Introduction vii

Program Chairman's Introduction ix

Programme Committee xi

Reviewers xi

Session Chairpersons xii

OA: Hardware and software in system engineering 1
Opening Address: D.Q.M. Fay

K1: Small and medium sized industries (SMI) 3
Keynote speaker: ir. G.A. Schwippert

K2: The strategic importance of microcomputing for the business environment 5
Keynote speaker: prof. ir. J.A. Dinklo

K3: Responsive systems (the challenge for the nineties) 9
Keynote speaker: prof. M. Malek

K4: The state of global printing in the '90s. 17
Keynote Speaker: Robert V. Adams

A1: RISC Systems 19
Session Chairman: J. Cortadella (E).

Architectural support for operating systems: a popular RISC vs a popular CISC 21
A.I. Karshmer (D).

A RISC central processing unit for a massively parallel architecture 33
F. Cappello, J.-L. Bechennec, D. Etiemble (F).

ASTRA: An associative RISC architecture 41
D. Tavangarian, M. Beck (D).

A2: Signal Processing - I 49
Session Chairman: N. Scarabottolo (I).

A DSP processor with a powerful set of elementary arithmetic operations based on CORDIC and CCM algorithms 51
D.E. Metafas, C.E. Goutis (GR).

A hardware implementation of a modified DES-algorithm 59
T. Kropf, J. Froessl, W. Beller, T. Giesler (D).

Computational logic unit for a microprogrammed data acquisition system: an evaluation prototype 67
W. Bragagnini, P. Guazzoni, M. Pitalieri, L. Zetta (I).

A3: Parallel Applications 75
Session Chairman: J. Tiberghien (B).

Dynamic load balancing in transputer applications with geometric parallelism 77
W. Joosen, Y. Berbers, P. Verbaeten (B).

An Occam-based evaluation of a parallel version of simulated annealing 85
V.C. Barbosa, M.C.S. Boeres (BR).

Occam implementation of path-disjoint routing on the Hathi-2 transputer system 93
Hong Shen (SF).

A4: System Design I 101
Session Chairman: H. Schumny (D).

PASS: High level synthesis 103
C. Ewering, G. Gerhardt (D).

The interactive space-time scheduler 109
B. Lisper (S).

Stepwise decomposition in controlpath synthesis 117
A.J.W.M. ten Berg (NL).

B1: VLSI Architectures 125
Session Chairman: H. Painke (D).

A 32-bit RISC CPU implemented in GaAs 127
W.A. Geideman, R.A. Niederland, D.A. Harrington (USA).

Designing high performance instruction caches in VLSI 135
J.E.H.M. Bormans, W.J. Withagen, F.P.M. Budzelaar, M.P.J. Stevens (NL).

Evaluation of the optimal strategy for managing the register file 143
O. Arregi, C. Rodríguez, A. Ibarra (E).

B2: Signal processing - II 151
Session Chairman: D. Wilson (UK).

Partitioned algorithms for Gaussian Elimination on reconfigurable processor arrays 153
M. Maresca, G. Carravieri, G. Cornara, A.L. Frisiani (I).

Design of a transputer network for searching neighbours in M.D. simulations 159
H. Bekker, M. Renardus (NL).

The IRCAM signal processing workstation - An environment for research in real-time musical signal processing and performance 167
E. Lindemann, M.Puckette, E. Viarra, M. Starkier (F).

B3: Formal Issues 175
Session Chairman: J. Mølgaard (DK).

The role of languages in the design-trajectory 177
R.J. Huis in 't Veld (NL).

Towards the verification of optimizing transformations for imperative programs 185
G. Kock (D).

Petri nets in logic 193
A. Domenici (I).

B4: Parallel Processing I 199
Session Chairman: F. Vajda (USA).

Towards a parallel inference machine: the APIM project 201
J. Vlahavas, A. Pombortsis, D. Stamatis (GR).

A new solution of coherence protocol for tightly coupled multiprocessor systems 207
C.A. Prete (I).

Distributed simulation of computer networks 215
E. Dirkx, F. Verboven, J. Tiberghien (B).

C1: VLSI Design I 221
Session Chairman: A. Nuñez (E).

Synthesis of programmable control structures for a simulation speed-up 223
J.-L. Dubois (F), P. Bakowski (F), A. Pawlak (D).

Quasi dynamic approach to layout compaction 231
S. Balakrishnan, S.K. Nandy (IND).

A generator for number format conversion IC 237
N.A. Kyrloglou, O.G. Koufopavlou, C.E. Goutis (GR).

An object oriented design and simulation system for VLSI 241
A.C. Verschueren (NL).

C2: Neural Networks 247
Session Chairman: G. Kock (D).

A cellular architecture dedicated to neural net emulation 249
B. Faure, G. Mazare (F).

System architecture of a modular neural network using 400 simple processors 257
J. Hoekstra (NL).

A case study in the migration of software to hardware using ASIC's 263
L. Spaanenburg, A.J. Beltman, J.A.G. Nijhuis, A. Reitsma (D).

C3: Software Engineering I 271
Session Chairman: J. Karjalainen (SF).

Solution in software crisis 273
A. Auer, M. Levento, A. Okkenen, J. Okkonen (SF).

CASE tool support for requirements capture and analysis 281
I. McChesney, D. Glass, J.G. Hughes (UK).

Statecharts based requirements analysis: deriving user oriented models 289
T. Jokela, K. Lindberg (SF).

Supporting testing of specifications and implementations 297
J. Arkko, V. Hirvisalo, J. Kuusela, E. Nuutila (SF).

D1: VLSI Design II 303
Session Chairman: K. Kuchcinski (S).

Simultaneous decompositions of sequential machines 305
L. Jóźwiak (NL).

Random logic cicuit implementation of extended time Petri nets 313
M.R.K. Patel (S).

System level VLSI design 321
M.P.J. Stevens, F.P.M. Budzelaar (NL).

D2: Image Processing I 331
Session Chairwoman: E. Pissaloux (F).

EIKON : A software library for image processing applications 333
K. Parthenis, C. Metaxaki-Kossionidis, B. Dimitriades (GR).

VOXEL based modeling and rendering irregular solids 341
C.E. Prakash, S.K. Nandy (IND).

A transputer based implementation of the VOXAR project 347
P. Pitot, B. Moisan, Y. Duthen, R. Caubet (F).

D3: Software Engineering II 355
Session Chairman: J. Karjalainen (SF).

Reverse engineering and data flow diagrams in ADA environment 357
G. Canfora, A. Cimitile, U. De Carlini (I).

An environment for parallel programming in PASCAL 365
N.Q. Vasconcelos, E.S.T. Fernades, F.M.B. Barbosa (BR).

Recovery meta program in UNIX based environment 371
A. Clematis, G. Dodero, V. Gianuzzi (I).

D4: Real Time Systems I 379
Session Chairman: W.A. Halang (NL).

Animation prototyping of formal specifications of real-time systems 381
T.S. Hughes, J.E. Cooling (UK).

The specification and design of hard real-time systems using timed and temporal Petri nets 389
J.S. Sagoo, D.J. Holding (UK).

A mixed implementation of a real-time system 397
C. André, L. Fancelli (F).

E1: VLSI Specification and Verification 403
Session Chairwoman: A. Antola (I).

An approach to a design for testability personal consultant 405
G. Buonanno, A. Burri, F. Fummi, D. Sciuto (I).

Assessing the diagnostic power of test pattern sets 413
P. Camurati, A. Lioy, P. Prinetto, M. Sonza Reorda (I).

The OTTER environment for resolution-based proof of hardware correctness 421
P. Camurati, T. Margaria, P. Prinetto (I).

E2: Image Processing II 429
Session Chairman: E. von Puttkamer (D).

Special architecture for high performance scan conversion 431
P.B. Franken, A.J. van de Goor (NL).

A parallel architecture for real-time video coding 439
L. de Sá, V. Silva, F. Perdigão, S. Faria, P. Assunção (P).

Application and implementation of window-based image processing algorithms 447
F. Vajda (USA).

E3: Compilation Issues 455
Session Chairman: P. Milligan (UK).

Designing a parallel object-oriented compiler target language (TOOL) 457
A.T. Balou, A.N. Refenes (UK).

From program to hardware: a parallel architecture compiler 467
M. Auguin, F. Boeri, C. Carriere, G. Menez (F).

Integrating intermediate code optimization with retargetable code generation 475
E. Accomazzo, M. Ancona, R. Bobbio, C. Cagnassi, L. Paolin (I).

E4: Real Time Systems II 483
Session Chairman: W.A. Halang (NL).

Constructing real-time multi-channel protocols 485
M. Kapus-Kolar (YU).

Real-time functional programming systems 491
S.C. Winter, D.R. Wilson, D.F. Neale (UK).

TAM: Temporal agent model for real-time distributed systems 499
D. Scholefield, H. Zedan (UK).

F1: Fault Tolerance and Testing 507
Session Chairman: F. Distante (I).

CMOS layout generation for improved testability 509
O. Stern, H.T. Vierhaus (D).

Experimental evaluation of a set of simple error detection mechanisms 513
H. Madeira, G. Quadros, J.G. Silva (P).

A bus-monitor unit for fault-tolerant system configurations 521
T. Markas, N. Kanopoulos (USA).

A transputer-based gate-level fault simulator 529
G. Cabodi, S. Gai, M. Sonza Reorda (I).

F2: System Design II 535
Session Chairman: K. Klockner (D).

On the formal specification and verification of digital circuits 537
P.J. de Graaff (NL).

An interactive environment for hardware/software system design at the specification level 545
S. Antoniazzi, M. Mastretti (I).

A rational methodology for design of new computer structures 555
E.E. Pissaloux (F).

Behavioral circuit description on system level 561
U. Wienkop (D).

F3: Parallel Software Development 567
Session Chairman: S. Winter (UK).

Co-programming: a tool for development of software for massively parallel computers 569
E.E. Pissaloux, S. Bouaziz, A. Merigot, F. Devos (F).

The COIN model for concurrent computation and its implementation 577
P. Buhler (D).

Data flow methods in the design of parallel computing systems 585
A.M. Tyrrell, G.F. Carpenter (UK).

Program development within the Mathematician's Devil 593
T.J.G. Benson, P. Milligan, N.S. Scott (UK).

G1: Parallel Processing II 599
Session Chairman: M.J. Taylor (UK).

Performance analysis of a multiprocessor machine based on data flow principles 601
R. Narayan, V. Rajaraman (IND).

Systolic architecture for the calculation of the correlation coefficients 609
E.L. Zapata, J.C. Cabaleiro, R. Doallo, F. Argüello (E).

A new comparison-based scheme for multiprocessor fault tolerance 617
Jie Xu, Shize Huang (CHN).

G3: Distributed Systems 625
Session Chairman: E. von Puttkamer (D).

TVNet II: A cable TV based metropolitan area network using the KEDS protocol 627
A.I. Karshmer, J.N. Thomas (USA), J.M. Phelan (D).

Join optimization in distributed databases on broadcast network 637
J.K. Ahn, S.C. Moon (ROK).

Message passing via singly-buffered channels: an efficient and flexible communications control mechanism 645
A.N. Refenes (UK).

H1: Parallel Processing III 655
Session Chairman: M.J. Taylor (UK).

Vector addressing processor for direct and indirect accesses 657
J.-L. Dekeyser, P. Marquet, P. Preux (F).

Pipelining a memory based CISC processor 665
J.P.C.F.H. Smeets, W.J. Withagen, M.P.J. Stevens (NL).

H2: System Design III 673
Session Chairman: S.-K. Jung (ROK).

A performance analysis of toroidal mesh networks 675
G.M. Macharia, J. Austin (UK).

Enhancing a control graph based HDL for performance evaluation of simulated architectures 683
R. Gajda, M. Thor, M. Tudruj (PL).

H3: Interprocess Communication 693
Session Chairman: G. Ciccarella (I).

The synthesis of deadlock-free interprocess communications 695
G.F. Carpenter (UK).

A deadlock-free communication kernel for loop connected message passing computer architecture 703
P. Pramanik (IND), P.K. Das (IND), A.K. Bandyopadhyay (IND), D.Q.M. Fay (UK).

Session Chairpersons' Addresses 713

Subject Index 715

Author Index 719